REMARKS

Page 8 of the description is amended.

Claims 1-8 are pending in the application. Claims 1, 3, 4 and 6 to 8 are amended.

Claim Rejections - 35 *USC* § 112

Claims 1-8 stand rejected under 35 USC 112, second paragraph as being indefinite. Applicant respectfully traverses the rejection.

Regarding claim 1

The Office Action states that " (…) the recitation "clock pulse generator apparatus comprising a clock pulse generator for generating a train of return-to zero primary clock pulses each having leading and trailing edges defining alternately an active clock phase and a non-active clock phase" is not clear" and states that "The "train of return-to zero primary clock pulses" is not seen in figure 5 and it is not clear how it is generated."

Applicant traverses this rejection. Claim 1 is amended to refer to 'a train of first clock pulses' instead of "a train of return-to zero primary clock pulses". Applicant submits that claim 1 is clear in this respect, at least as amended.

Figure 5 shows as an input clock signal a series of clock pulses, denoted with CLK. In this respect, it is observed that the term "train" is commonly used in the art to refer to a series of clock pulses, see as a non-limiting example for instance *http://en.wikipedia.org/wiki/Pulse_wave*. The clock input signal CLK of the clock generator shown in Figure 5 can be generated by any suitable source, as stated at page 7 line 28. Such suitable sources are well known to those skilled in the art. Thus, the "train of first clock pulses' as recited in claim 1 as a train of first clock pulses is shown in Figure 5 and it will be clear how they are generated.

Claim 1 has been amended to meet the objections to the expressions "a delay module", "a combiner" and "the primary clock pulse".

The Office Action states that "said continuous-time sigma-delta modulator being connected to utilize said train of combined clock pulses as clock" is confusing. Applicant traverses this rejection. FIGs. 1 and 2 show generic examples of continuous-time sigma-delta modulators (see p.4 l.4: Figure 1 shows the general scheme of a CT signal delta modulator (…)

and p.4 l.26: Figure 2 shows the general scheme of a continuous time digital to analog converter comprising a digital signal delta modulator (…).

To avoid any misunderstanding, Applicant refers to page 7 line 10, which states "this embodiment of the invention focuses on attenuating jitter within the clock signal before it is applied to the circuit". Thus, it will be clear that if the circuit of FIG. 5 is used in the generic examples of FIGs. 1 and 2, the circuit of FIG. 5 is provided between the source of the jittery clock signal and the clock input of the respective element in FIG. 1 and 2, and provide the output, the train of return-to-zero clock pulses CLK_JF to the clock input of the respective element in FIG. 1 and 2 instead of the jittery clock signal CLK.

Applicant submits that for the reasons above FIGs. 1 and 2 are entirely consistent with FIG. 5 and that there is no confusion with respect to "said continuous-time sigma-delta modulator being connected to said combiner to utilize said train of return-to-zero clock pulses as clock" as recited in claim 1.

Regarding claim 3

The Office Action states "figure 9 shows that circuit (22) receives the "jitter clock input signal" CLK and this clock is not the "said train of primary clock pulse" as recited." Applicant submits that Figure 9 correctly shows the (jittery) clock input signal CLK as input to the circuit 22 and that this input signal is indeed the same input signal as applied to the circuit 14, the 'first series of delay elements' of claim 2.

Claim 3 has been amended to clarify which plurality of clock periods are used for averaging the adjustment signal. Applicant submits that, at least with this amendment, no risk of confusion exists and that the rejection is traversed.

Regarding claim 4

Claim 4 has been amended to specify "said substantially identical delay elements". Applicant submits that, at least with this amendment, no risk of confusion exists and that an antecedent basis for this recitation is present in claim 2.

Regarding claim 5

Applicant observes that claim 1 reads onto both figure 1 and 2. Although Applicant submits that claim 5 does not read on FIG. 1 only, claim 5 reading on FIG. 1 is not inconsistent with claim 1 reading on both FIG. 1 and 2.

The Office Action states that claim 1 "reads onto Figure 2" and that "figure 1 does not have the "delay module" recited in claim 1." As submitted in the Pre-Appeal Brief Statement of February 18th 2009, Applicant submits that the specification clearly describes that the invention utilizes the clock generator of Figure 5 (which does have the "delay module") to generate the clock signals for the continuous-time sigma-delta modulator of Figure 1 or 2 and that claim 1 is directed to the combination of a continuous-time sigma-delta modulator with the clock pulse generator recited.

Applicant respectfully submits that claim 1 recites "[a]pparatus for converting between analogue and digital signals (…)" which reads onto both the kind shown in Figure 1 and the kind shown in Figure 2. As stated on p.10 l.28 - p.11 l. 1 the paragraph bridging pages 10 and 11, "the clock pulse generator with a substantially jitter-free active phase (…) applies to both sigma delta ADCs and DACs." Thus, claim 1 reads on both figure 1 and 2

Furthermore, sigma-delta modulators of both kinds shown in Figures 1 and 2 may include integrators. Applicant refers to the passage on page 6 at lines 24 to 26 "the first stage of digital to analog CT sigma delta modulators is a continuous time integrator (for example, the low pass filter of a digital to analog CT sigma delta)". Applicant submits that this passage is consistent with the presence of an integrator in the filter 10 of Figure 2 and that claims 1 and 5 cover embodiments of the invention of the kind shown in Figure 2 as well.

As claims 1 and 5 cover embodiments of the invention of the kind shown in Figure 1 as well as Figure 2, Applicant submits that claim 5 is clear is clear in these respects.

Regarding claim 6

The Office Action states that claim 1 "reads onto Figure 2". Applicant again respectfully submits that claim 1 covers "Apparatus for converting between analogue and digital signals" both of the kind shown in Figure 1 and of the kind shown in Figure 2. As stated in the paragraph bridging pages 10 and 11, "the clock pulse generator with a substantially jitter-free active phase" … "applies to both sigma delta ADCs and DACs."

The Office Action states "figure 1 shows that the digital-to-analog converter module (5) whose operation is responsive to the "jitter clock input signal CLK", not the "said train of combined clock pulses" (CLK_JF) as recited". However, Applicant submits that Figures 1 and 2 show generically the sigma-delta modulator as receiving a clock signal, not specifically a jittery clock signal. Applicant refers to page 7 line 10, which states "this embodiment of the invention focuses on attenuating jitter within the clock signal before it is applied to the circuit".

Applicant submits that claim 6 is clear in these respects.

Regarding claim 7

The Office Action states "Claim 7 is confusing because claim 7 depends upon claim 1. Claim 1 reads on figure 2. the "input for receiving said analog signal" and "an output for said digital signal" are on figure 1."

Applicant again respectfully submits that claim 1 covers "Apparatus for converting between analogue and digital signals" both of the kind shown in Figure 1 and of the kind shown in Figure 2. Applicant submits that no risk of confusion exists because claim 7 recites "input for receiving said analogue signal, an output for said digital signal".

Claim 7 is amended for consistency with claim 6 from which it depends.

Regarding claim 8

The Office Action states "Regarding claim 8, the recitation "wherein said continuous-time sigma-delta modulator comprises an input for receiving said digital signal and an output for said analogue signal, said digital-to-analogue -module being in series between said input and said output" is confusing because figure 1 shows that the continuous-time sigma-delta modulator receives an analog input signal (X) and outputs a digital signal (Y)".

Applicant submits that claim 8 clearly is supported by Figures 2 and 5. Applicant submits that no risk of confusion exists because claim 8 recites "an input for receiving said digital signal and an output for said analogue signal".

The Office Action states "The Applicant is requested to select one of the two distinct drawings, figure 1 or figure 2 for claims 1-8." Applicant submits that the application includes an allowable claim, such as claim 1, generic to claims 7 and 8 and generic to Figures 1 and 2, and

that claims 7 and 8 are written in dependent form. Applicant submits that no statutory requirement for selection of Figure 1 or Figure 2 exists.

Claim 8 is amended for consistency with claim 6 from which it depends.

***Claim Rejections* - 35 *USC* § 103**

Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Di Giandomenico (US 7,486,214) in view of Kim (US 7,358,786) and Tachimori (US 6,603,340).

Di Giandomencio (US 7,486,214) was filed on Sept 4, 2007 which was after the US filing date of this application: May 26th 2006.

Kim (US7358786) was filed on November 17, 2005. This is after the PCT filing date of this application November 26th 2004. Applicant is filing an amended Application data sheet to claim domestic priority to the PCT filing.

Because the filing date of this application is prior to the references dates of the Di Giandomenico and Kim, the obviousness rejection set forth in this Office Action is improper. Accordingly, claims 1-8 are nonobvious over Di Giandomenico, Kim, and Tachimori .

Although Applicants may disagree with statements made by the Examiner in reference to the claims and the cited references, Applicants are not discussing all these statements in the current Office Action since reasons for the patentability of each pending claim are provided without addressing these statements. Therefore, Applicants reserve the right to address these statements at a later time if necessary.

No amendment made herein is related to the statutory requirements of patentability unless expressly stated herein. Further, no amendment herein is made for the purpose of narrowing the scope of any claim, unless Applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079.

Respectfully submitted,

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